**Activity - 1  
Question 1 (10 marks)**

Figure below shows a memory circuit of a microprocessor interfaced with two memory chips (1 and 2). As indicated in the figure, the microprocessor has 16 address lines A0 to A15, 8 data line D0 to D7. Further, as seen in the figure a few of the address lines are combined using suitable logic circuit and connected to the chip select (CS) pin of the memory chips. Answer the questions raised in the Table 1.

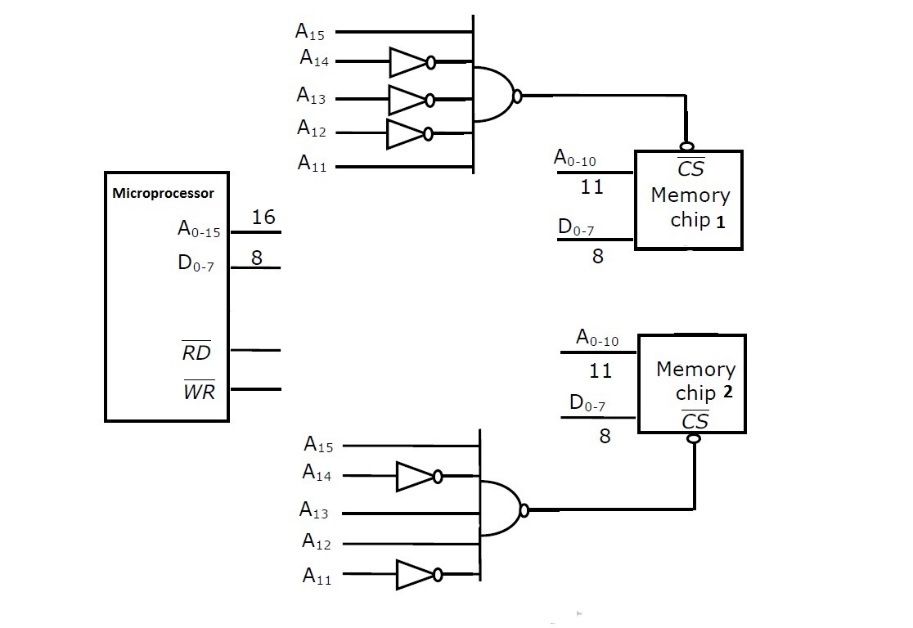


Figure 1.

Table 1.

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| --- | --- |
| Question | Answer |
| The starting address of Chip 1:  (2 marks) | 0x8800 |
| The Ending address of Chip 1:  (2 marks) | 0x8FFF |
| The starting address of Chip 2:  (2 marks) | 0xB000 |
| The ending address of Chip 2:  (2 marks) | 0xB7FF |
| Total memory size of the circuit  (2 marks) | (2^11) \* 2 bits => 4096 bytes |

**Question 2 (6 marks)**

Figure below shows memory cells in Dynamic RAM circuit where the capacitors (C) in each cell stores the digital value in form of charge. Answer the following questions:

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**Question (a)**

Clarify how the same column ‘bit sense lines’ is used for both read and as well as to write a bit value into a particular memory cell (5 marks)

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**Question (b)**

Answer in a sentence, how DRAM overcomes leakage of capacitor charge and retains the digital value stored in a memory cell. (3 marks)

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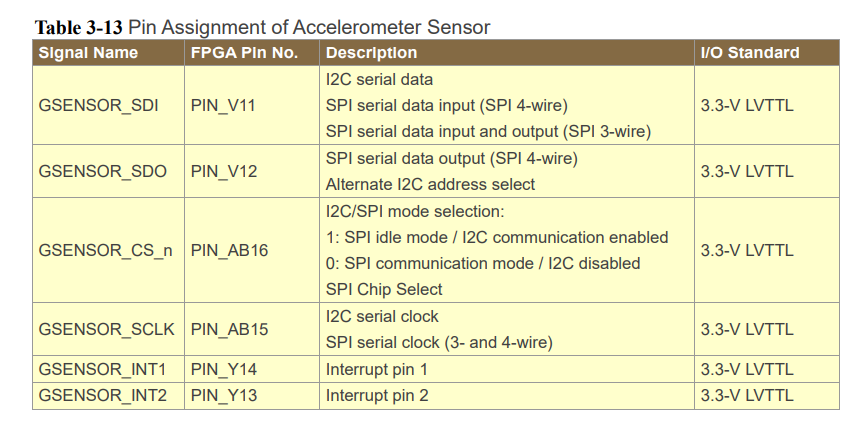
**Question 3**

**Identify the accelerometer details in DE10 board and list the SPI pins Identify the SPI pins for interfacing.**

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**Question 4**

**Identify the SD RAM chip in DE10 board**

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**Question 5**

**How tristate buffer and D-Flip Flop aid in data communication between peripherals and CPU**

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**Question 6**

**Using DE10 lite board and Chapter 4 of DE10 lite Manual (**[**pdf here**](https://ftp.intel.com/Public/Pub/fpgaup/pub/Intel_Material/Boards/DE10-Lite/DE10_Lite_User_Manual.pdf)**) demonstrate built-in accelerometer and SPI communication**

**Question 7**

**Show how you will include the accelerometer interface via SPI.**

**Activity 2 : Refer to the UART exercise sheet attached and demonstrate serial communication.**